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Education :

Ph.D., Electrical Engineering, University of Maryland, 1988.
Dissertation: Characterization and Modeling of Localized Hot-Carrier- Induced Charge Effects in Microelectronic Switching Circuits.

MSEE, Thesis Option, University of Maryland, 1982.
Thesis: An Experimental Study of Wafer Level Acceptance Testing Based on Sampling Test Chip Data.

BSEE, University of Maryland, 1980.

Employment :

1982-present: National Institute of Standards and Technology, Gaithersburg MD. Project Leader for Advanced MOS Characterization and Reliability research effort. Responsible for planning and conducting research to characterize, monitor, and improve semiconductor reliability by developing and evaluating methods, tools, diagnostic procedures, data, and models for understanding wear-out and breakdown phenomenon in ultra-thin silicon dioxide and alternative gate dielectric films.. Other activities included developing micromachined thermally isolated micro-hotplate structures for integrated chemical sensor arrays and developing test structures for characterizing molecular electronic devices.

1980-1982: University of Maryland/NIST Graduate Fellowship, University of Maryland, College Park MD. Developed testing techniques and statistical analysis for obtaining a minimum sample size for characterizing microelectronic parametric test data. Was responsible for managing and developing software for a parametric test system.

Honors/Awards:

University of Maryland/NIST Graduate Research Fellowship, 1980-1982
Department of Commerce Bronze Medal Award, 1994, For "Developing Methods for Testing Semi-conductor Device Oxides to Improve the Modeling of Devices Under Stress Test to Reduce Test Times"
Outstanding Paper Award, 1994 International Reliability Physics Symposium
Best Paper Award, 1995 International Reliability Physics Symposium
Best Paper Award, 1996 International Reliability Physics Symposium
Senior Member of IEEE
Special Member of Graduate Faculty of the University of Maryland 1996-2001

Professional Activities:

Member of EKN, US Citizenship, Secret Clearance
Chairman of Dielectric Integrity Working Group for EIA-JEDEC 14.2 Committee on Wafer-Level Reliability Technical Program Committee, IEEE International Integrated Reliability Workshop
Technical Program Committee 1996-1997, IEEE International Electron Device Meeting
Technical Program Chairman, 2006, IEEE International Reliability Physics Symposium
Technical Program Committee, 2000-present, Process and Plasma Induced Damage Conference
Guest Editor IEEE Transactions on Materials and Device Reliability 2005

Patents:

``Temperature-Controlled , Micromachined Arrays for Chemical Sensor Fabrication and Operation", Sept. 6, 1994, US patent No. 5,345,213

``Application of Microsubstrates for Material Processing", Oct. 18,1994, US patent No. 5,356,756

``Micro-Hotplate by CMOS Technology with Applications for Sensors, In-Situ Processing, and Process Monitoring", Nov. 7, 1995, US patent No. 5,464,966

“Micron Scale Differential Scanning Microcolorimeter on a Chip” June 27, 2000, US patent No. 6,079,873

Tutorials/Short Courses Presented:

J. S. Suehle, C. Messick, and, B. Langley, “Practical Monitoring and Characterization of Thin Dielectrics”, Tutorial at International Reliability Physics Symposium, Apr. 3, 1995.

J. S. Suehle, and E. M. Vogel, ‘Thin Gate Oxide Reliability,’ Tutorial at International Reliability Physics Symposium, Apr. 10, 2000.

J. S. Suehle, "Thin Gate Oxide Reliability: Physics, Statistics, and Models," University of New Mexico Microelectronics Reliability Seminar Series, Albuquerque, NM, March 2, 2000.

J. S. Suehle, “Ultra-Thin Gate Oxide Reliability and Implications for Design”, Tutorial at the 2002 IEEE International Conference on Quality Electronic Design, San Jose, CA, March 18, 2002.

J. S. Suehle,” Reliability Characterization and Projection Issues of Advanced Gate Dielectrics” Portland Area Semiconductor Seminar Series, Portland State University, March 15, 2002.

J.S. Suehle,” Molecular Electronics: What will be the Reliability Issues?, 2002 Integrated Reliability Workshop, Lake Tahoe, CA, October 22, 2002 .

J. S. Suehle, “Potential Reliability Issues for Molecular Electronics,” The Aerospace Corporation. Los Angeles, CA December 5, 2002.

J.S. Suehle, “ Advanced Dielectric Reliability Characterization”, Reliability Engineering Department Seminar, University of Maryland , March 3, 2003

J.S. Suehle, “ Molecular Electronics”, Reliability Engineering Department Seminar Series, University of Maryland , April 29, 2003

J. S. Suehle “Reliability Year In Review: Gate Dielectrics”, 2004 International Physics Symposium, Phoenix, AZ.

J. S. Suehle, “Reliability Challenges for Advanced Semiconductor Devices”, SEMICON West, San Francisco Ca on July 11, 2005.

Professional Publications/Presentations:

J. S. Suehle, L. W. Linholm, and G. M. Marshall, ``Evaluation of a CMOS/SOS Process Using Process Validation Wafers", NBSIR 82-2514, 1982.

J. S. Suehle, L. W. Linholm, and K. Kafadar, ``Minimum Test Chip Sample Size Selection for Characterizing Process

Parameters", *IEEE Trans. on Electron Devices*, ED-31, p.257, 1984.

J. S. Suehle, L. W. Linholm, and K. Kafadar, "Minimum Test Chip Sample Size Selection for Characterizing Process Parameters", *IEEE Journal of Solid State Circuits*, SC-19, p.122, 1984.

H. S. Bennett, M. Gaitan, P. Roitman, T. J. Russell, and J. S. Suehle, "Modeling MOS Capacitors to Extract SiO₂-Si Interface Trap Densities in the Presence of Arbitrary Silicon Doping Profiles", *IEEE Trans. on Electron Devices*, ED-33, p.257, 1986.

T. J. Russell, H. S. Bennett, M. Gaitan, J. S. Suehle, and P. Roitman, "Correlation Between CMOS Transistor and Capacitor Measurements of Interface Trap Spectra", *IEEE Trans. Nuc. Sci.*,NS-33, p.1228, 1986.

J. S. Suehle, T. J. Russell, and K. F. Galloway, "Interface Trap Effects on the Hot-Carrier Induced Degradation of MOSFETs During Dynamic Stress", *IEEE Trans. Nuc. Sci.*,NS-34, p.1359, 1987.

J. S. Suehle and K. F. Galloway, "The Effects of Localized Hot-Carrier induced charge in VLSI Switching Circuits", *Microelectronics Journal*, Vol. 21, No. 3, pp 5-14, 1990

J. S. Suehle and H. A. Schafft "Techniques and Characterization of Pulsed Electromigration at the Wafer level", *Microelectronics and Reliability*, Vol.32, No. 11, pp. 1527-1532, 1992.

S. C. Witczak, J. S. Suehle, and M. Gaitan, "An Experimental Comparison of Measurement Techniques to Extract Si-SiO₂ Interface Trap Density", *Solid State Electronics (Invited)*, Vol. 35, No. 3, pp. 345-355, 1992.

H. A. Schafft and J. S. Suehle, "The Measurement, Use, and Interpretation of the Temperature Coefficient of Resistance of Metallizations," *Solid State Electronics (Invited)*, Vol. 35, No. 3, pp. 403-410, 1992.

J. S. Suehle, R. E. Cavicchi, M. Gaitan, and S. Semancik, " Tin Oxide Gas Sensor Fabricated Using CMOS Micro-Hotplates and In-Situ Processing", *IEEE Electron Device Letters*, Vol.14, No. 3, pp. 118-120, 1993.

J. S. Suehle, L. W. Linholm, and K. Kafadar, "A Method for Selecting a Minimum Test Chip sample Size to Characterize Microelectronic Process Parameters", *Proc. 1983 Custom Integrated Circuits Conf.*, Rochester, NY., May 23-25, p.308, 1983.

P. Roitman, J. S. Suehle, T. J. Russell, and M. Gaitan, "On the Measurement of Capacitance on Wafers", *Proc. IEEE VLSI Workshop on Test Structures*, Long Beach, CA., February 17-18, 1986.

J. S. Suehle and K. F. Galloway, " Test Circuit Structures for Characterizing the Effects of Localized Hot-Carrier-Induced Charge in VLSI Switching Circuits", *Proceedings of the IEEE International Conference on Microelectronic Test Structures*, Long Beach, CA., Feb. 22-24, 1988.

H. A. Schafft, J. S. Suehle, and P. G. Mirel, "Thermal Conductivity Measurements of Thin-Film Silicon Dioxide", *Proceedings of the IEEE International Conference on Microelectronic Test Structures*, Edinburgh, Scotland, March 13-14, 1989.

J. S. Suehle and H. A. Schafft, "The Electromigration Response Time and Implications for DC and Pulsed Characterizations", *International Reliability Physics Symposium Technical Digest*, Phoenix, Arizona, April 10-13, pp. 229-233, 1989.

J. S .Suehle and H. A. Schafft, "Current Density Dependence of Electromigration t50 Enhancement Due to Pulsed Operation", *International Reliability Physics Symposium Technical Digest*, New Orleans, Louisiana, March 27-29, pp. 106-110, 1990.

M. Gaitan, M. Parameswaren, M. Zaghloul, J. Marshall, D. Novotny, and J. S. Suehle, "Design Methodology for Micromechanical Systems at Commercial CMOS Foundries Through MOSIS", *Proc. 35th Midwest Symposium on*

Circuits and Systems, Washington DC, August 1992.

J. S. Suehle and M. Gaitan, ``Application of CMOS-Compatible Micro-Hotplates for In-Situ Process Monitors," *International Wafer-Level Reliability Workshop Final Report*, Lake Tahoe, CA, October 25-28, pp. 122-132, 1992.

S. Mayo, J. S. Suehle, and P. Roitman, ``Breakdown Mechanism in Buried Silicon Oxide Films", *Journal of Applied Physics*, Vol. 74, No. 6, p.4113, 1992.

S. C. Witczak, M. Gaitan, J. S. Suehle, M. C. Peckerar, and D. I. Ma, "The Interaction of Stoichiometry, Mechanical Stress, and Interface Trap Density in LPCVD Si-Rich $\text{SiN}_x\text{-Si}$ Structures", *Solid State Electronics*, Vol. 37, No.10, p. 1695, 1994.

J. S. Suehle, "Reproducibility of JEDEC Standard Current and Voltage Ramp Test Procedures for Thin-Dielectric Breakdown Characterization," *Integrated Reliability Workshop Final Report*, Lake Tahoe, CA, p.22, 1993.

J. S. Suehle, P. Chaparala, C. Messick, W. M. Miller, and K. C. Boyko, "Experimental Investigation of the Validity of TDDB Voltage Acceleration Models," *Integrated Reliability Workshop Final Report*, Lake Tahoe, CA, p.59, 1993.

J. S. Suehle, P. Chaparala, C. Messick, W. M. Miller, and K. C. Boyko, "Field and Temperature Acceleration of Time-Dependent Dielectric Breakdown in Intrinsic Thin SiO_2 ," *International Reliability Physics Symposium Technical Digest*, April 12-14, pp.120-125, 1994.

J. S. Suehle, P. Chaparala, and C. Messick, "High Temperature Reliability of Thin Film SiO_2 ", *Transactions of 2nd International High Temperature Electronics Conference*, Charlotte, NC, June 5-10, Vol. 1, p.VIII-15, 1994.

R. E. Cavicchi, J. S. Suehle, P. Chaparala, G. Poirier, K. Kreider, M. Gaitan, and S. Semancik, "Microhotplate Temperature Control for Sensor Fabrication, Study, and Operation," *Proceedings of the Fifth International Meeting on Chemical Sensors*, Rome, Italy, July 11-14, pp. 1136-1139, 1994.

R. Cavicchi, J. S. Suehle, P. Chaparala, K. Kreider, M. Gaitan, and S. Semancik, "Micro-hotplate Gas Sensor" *Proceedings of the Workshop on Sensors and Actuators*, Hilton Head, SC, June 13-16, pp. 53-56, 1994.

J. S. Suehle and P. Chaparala, "Characterization of Time Dependent Dielectric Breakdown in Intrinsic Thin SiO_2 ," *6th ESPiRiT Workshop on the Growth and Characterization of Thin Dielectrics* (Invited), Nov 23, 1995.

J. S. Suehle and P. Chaparala, "Time Dependent Dielectric Breakdown in Thin Intrinsic SiO_2 Films," *Materials Research Society Spring Meeting Technical Digest* (Invited), April 17-21, 1995.

R. E. Cavicchi, J. S. Suehle, P. Chaparala, K. G. Kreider, B. L. Shomaker, J. A. Small, and M. Gaitan, "Growth of SnO_2 Films on Micromachined Hotplates", *Appl. Phys. Letters*, 66. No. 7, p.812, 1995.

J. Prendergast, J. S. Suehle, P. Chaparala, E. Murphy, and M. Stephenson, "TDDB Characterization of Thin SiO_2 Films With Bimodal Failure Populations," *International Reliability Physics Symposium Technical Digest*, No. 33, pp. 124-130, 1995.

E. I. Cole, J. S. Suehle, K. A. Peterson, P. Chaparala, A. N. Campbell, E. S. Synder, and D. G. Pierce, "OBIC Analysis of Stressed, Thermally-Isolated Polysilicon Resistors," *International Reliability Physics Technical Digest*, No. 33, pp. 234-243, 1995.

R. E. Cavicchi, J. S. Suehle, K. G. Kreider, M. Gaitan, and P. Chaparala, "Fast Temperature Programmed Sensing for Micro-Hotplate Gas Sensors", *IEEE Electron Device Letters*, Vol. 16, No. 6 pp. 286-288, 1995.

R.E. Cavicchi, J. S. Suehle, K. E. Krieder, M. Gaitan, and P. Chaparala, "Optimized Temperature Pulse Sequence for the Enhancement of Chemically-Specific Response Patterns from Micro-hotplate Gas Sensors," *Proceedings of the Transducers 95/Eurosensors IX*, Stockholm, Sweden, pp. 823-826, 1995.

S. Semancik, R. E. Cavicchi, J. S. Suehle, K. E. Krieder, and P. Chaparala, Selected Area Deposition of Multible Active Films for Conductometric Microsensor Arrays," Proceedings of the Transducers 95/Eurosensors IX, Stockholm, Sweden, pp. 831-834, 1995.

S. Semancik, R. E. Cavicchi, F. DiMeo, G.E. Poirier, J. S. Suehle, and P. Chaparala, "Materials Issues for Conductive Microsensor Arraya," 210th American Chemical Society National Meeting, Chicago, August 1995.

S. Semancik, F. DiMeo, R. E. Cavicchi, J. S. Suehle, and P. Chaparala, "Microsensor Array Fabrication Using Self-Lithographic CVD on CMOS Microhotplates," 42nd National Symposium of the American Vaccum Society, October, 1995.

J. S. Suehle and P. Chaparala, "Low Electric Field Breakdown of Thin SiO₂ Films Under Static and Dynamic Stress," *IEEE Trans. on Electron Devices*, vol. 44, No. 5, p. 801 1997.

Y Chen, J. S. Suehle, C. C. Shen, J. Bernstein, C. Messick, and P. Chaparala, "A New Technique to Extract TDDB Acceleration Parameters from fast Qdb Tests," *International Integrated Reliability Workshop* Final Report, Oct 13-16, 1997, Lake Tahoe, CA. p. 67.

Y Chen, J. S. Suehle, C. C. Shen, J. Bernstein, C. Messick, and P. Chaparala, "The Correlation of Highly Accelerated Q_{bd} Tests to TDDB Life Tests for Ultra-Thin Gate Oxides," *International Reliability Physics Symposium Technical Digest*, No. 36, p87, 1998.

Y. Chen, J. S. Suehle, C-C. Shen, J. B. Bernstein, C. Messick, and P. Chaparala, "A New Technique for Determining Long-Term TDDB Acceleration Parameters of Thin Gate Oxides, IEEE Electron Dev. Lett, Vol. 19, No.7, P. 219, 1998.

H. A. Hoff, G. L. Waytena, C.L. Vold, J. S. Suehle, I.P. Isaacson, M. L. Rebbert, D. I. Ma, and K. Harris, "Ohmic Contacts to Semiconducting Diamond Using Ti/Pt/Au Trilayer Metallization Scheme," *Diamond and Related Materials*, vol. 26, no.2, p.1450, 1996.

A. Martin, J. S. Suehle, P. Chaparala, P. O'Sullivan, and A. Mathewson, "A New Oxide Degradation Mechanism for Stresses in the Fowler-Nordheim Tunneling Regime, Proceeding of the International Reliability Physics Symposium, Dallas TX, April 30-May 2, p. 67, 1996.

B. Schlund, J. S. Suehle, C. Messick, and P. Chaparala, "A New Physics-Based model for Time-Dependent Dielectric Breakdown", Proceeding of the International Reliability Physics Symposium, Dallas TX, April 30-May 2, p. 84, 1996.

G. L. Waytena, H.A. Hoff, I.P. Isaacson, L. Rebbert, D. I. Ma, C. Marrian, and J. S. Suehle, "The Optimization of the Double Mask System to Minimize the Contact Resistance of a Ti/Pt/Au Contact," *Journal of Electronic Materials*, vol. 26, no. 2, p. 90, 1997.

J. Kolodzy, E. A. Chowdhury, J. Olowolafe, C.P. Swann, K. M. Unruh, J. S. Suehle, R. G. Wilson, J. M. Zavada, "The effects of Oxidation Temperature on the Capacitance-Voltage Characteristics of Oxidized AlN Films on Si," *Appl. Phys. Lett.*, 71 (26), p. 3802, 1997.

J. Kolodzey, E. A. Chowdhury, T. N. Adam, Q. Guohua, I. Rau, J. O. Olowolafe, J. S. Suehle, and Y. Chen, "Electrical Conduction and Dielectric Breakdown in Aluminum Oxide Insulators on Silicon", *IEEE Trans. on Electron Dev.*, Vol. 47 pp. 121-128 , Jan. 2000.

J. S. Suehle, "Ultra-Thin Film Dielectric Reliability Characterization," *Gate Dielectric Integrity: Material, Process, and Tool Qualification*, ASTM STP 1382, D. C. Gupta and G. A. Brown. Eds., American Society for Testing and Materials, West Conshohocken, PA, 2000.

E. M. Vogel, J. S. Suehle, M. D. Edelstein, B. Wang, Y. Chen, and J. B. Bernstein, 'Reliability of Ultra-thin Silicon Dioxide Under Combined Substrate Hot Electron and Constant Voltage Tunneling Stress,' *IEEE Trans. Elec. Dev*, vol. 47, p. 1183, 2000.

E. M. Vogel and J. S. Suehle, 'Degradation and Breakdown of Ultra-thin Silicon Dioxide Induced by Substrate Hot Hole Injection,' 31st IEEE Semiconductor Interface Specialists Conference, San Diego, CA, Dec. 7-9, 2000.

J. Suehle, "Reliability Characterization and Projection Issues of Sub-3 nm Gate Oxides," Electronics Materials Conference, University Denver, Denver, CO, June 22, 2000.

Suehle, J. S., Vogel, E. M., Wang, B., and Bernstein, J. B., "Temperature Dependence of Soft Breakdown and Wear-Out in Sub-3 nm SiO₂ Films," Proceeding of the International Reliability Physics Symposium, San Jose, CA, April 10-13, 2000, p. 174.

B. Wang, J. S. Suehle, E. M. Vogel, and J. B. Bernstein, "Time-dependent Breakdown of Ultra-Thin SiO₂ Gate Dielectrics Under Pulsed Biased Stress", *IEEE Electron Dev. Lett*, Vol. 22, No.5, P. 224, 2001.

J.S. Suehle, B. Wang, J.F. Conley, Jr., E. M. Vogel, P. Roitman, C.E. Weintraub, A. H. Johnston, and J.B. Bernstein, 'Observation of Latent Reliability Degradation in Ultra-Thin Oxides After Heavy-Ion Irradiation,' *Appl. Phys. Lett.*, vol 80, no. 6, (2002).

Vogel, E. M., Edelstein, M. D., and Suehle, J. S., Defect Generation and Breakdown of Ultra-Thin Silicon Dioxide Induced by Substrate Hot Hole Injection, *Journal of Applied Physics*, v. 90, no. 5, September 1, 2001, pp. 2338-2347.

Vogel, E. M., Edelstein, M. D., and Suehle, J. S., Defect Generation and Breakdown of Ultra-Thin Silicon Dioxide Induced by Substrate Hot Hole Injection, *Journal of Applied Physics*, v. 90, no. 5, September 1, 2001, pp. 2338-2347.

Vogel, E. M., Edelstein, M. D., and Suehle, J. S., Reliability of Ultra-Thin Silicon Dioxide Under Substrate Hot-Electronic, Substrate Hot-Hole, and Tunneling Stress, *Microelectronics Engineering* 1 (2001), 11 p.

J. F. Conley, Jr., J. S. Suehle, A. H. Johnston, B. Wang, T. Miyahara, E. M. Vogel, and J. B. Bernstein, 'Heavy Ion Induced Soft Breakdown of Thin Gate Oxides,' *IEEE Trans. Nucl. Sci.* Dec. 2001.

J. S. Suehle, INVITED REVIEW PAPER: "Ultra-Thin Gate Oxide Reliability: Physical Models, Statistics, and Characterization, *IEEE Tran. On Elec. Dev.*, Vol. 29, No. 6, June 2002.

M.Y. Afridi, J.S. Suehle, M.E. Zaghoul, D. W. Berning, A.R. Hefner, R. E. Cavicchi, S. Semancik, C. B. Montgomer, and C. J. Taylor, "A Monolithic CMOS Microhotplate-based gas Sensor System," *IEEE Sensors Journal*, Vol. 2, No. 6. pp. 644-655 (01-DEC-2002)

J. S. Suehle (Invited), "Ultra-Thin Gate Oxide Reliability and Implications for Qualification, Design, and Use in Ionizing Radiation Environments, NASA Microelectronics and Qualification Workshop, Manhattan Beach, CA, December 2, 2002.

B. Zhu, J. S. Suehle, Y. Chen, J. B. Bernstein, "negative Bias Temperature Instability in Deep Sub-Micron p-MOSFETs Under Piulsed Bias Stress, " Proc. Integrated Reliability Workshop, Oct 21-24, 2002, Lake Tahoe, CA, p. 125, 2002..

J.-P. Han, E. M. Vogel, E.P. Gusev, C. D'Emic, C.A. Richter, D. W. Heh, J. Suehle, "Energy Distribution of Interface Traps in High-K Gated MOSFETs, 2003 VLSI Tech. Symp, Royal Hotel Kyoto Kyoto, Japan June 10-12, (2003)

J. S. Suehle (Invited) "Long-Term Reliability Projection Issues for Ultra-Thin Gate Dielectrics" Workshop on Aging and Long-Term Reliability of Microelectronics Materials and Devices, Vanderbilt University, October 9-10, 2003

(Invited) J. Suehle, "Reliability Implications of Scaling Gate Oxides in Deep Submicron CMOS Technologies," 2004 GOMACTech, Monteray, CA 2004.

(Invited) J. Suehle, "Ultra-Thin Gate Oxide Breakdown: A Failure That We Can Live With", Electronic Device Failure Analysis, vol. 6, no. 1, February 2004.

J. S. Suehle, B. Zhu, Y. Chen, and J. B. Bernstein" Acceleration Factors and Mechanistic Study of Progressive Breakdown in Small Area Ultra-Thin Gate Oxides," 2004 IRPS, Phoenix AZ, 2004.

B. Zhu, J. S. Suehle, and J. B. Bernstein, "Mechanism for Reduced NBTI Effect Under Pulsed Bias Stress Conditions Mechanism," 2004 IRPS, Phoenix, AZ, 2004.

J.-P. Han, E.M. Vogel, E.P. Gusev,C. D'Emic, C.A. Richter, D.W. Heh, J.S. Suehle, "Asymmetric Energy Distribution of Interface Traps in n- & p- MOSFETs with HfO₂ Gate Dielectric on Ultra-thin SiON Buffer Layer," IEEE Electron Device Letters, March 2004.

(Invited) J. S. Suehle, B. Zhu, Y. Chen, and J. B. Bernstein, Detailed Study and projection of Hard Breakdown Evolution in Ultra-thin gate Oxides, Microelectronics Reliability, 45, p. 419 2005.

S. Sayan, T. Emge, E. Garfunkel, X. Zhao, L. Weilunski, R. A. Bartynski, D. Vandebilt, J. S. Suehle, S. Suzer, M. and Banaszak-Holl, "Band Alignment issues related to HfO₂/SiO₂/p-Si Gate Stacks," J. Appl. Phys. vol.96, No. 12, p. 7485 2004.

B. Zhu, J. S. Suehle, and J. B. Bernstein, "The Contribution of HfO₂ Bulk Oxide Traps to Dynamic NBTI in pMOSFETs , " 2005 IRPS, San Jose, CA 2005.

B. Zhu, J. S. Suehle, and J. B. Bernstein, "Mechanism of Dynamic NBTI of pMOSFETs", Proceedings IEEE Integrated Reliability Workshop, Oct 18-21, 2004.

J. S. Suehle, "Reliability Challenges for Advanced Gate Dielectrics and Implications for Lifetime Projection," 2004 Microelectronics Reliability Qualification Workshop, Manhattan Beach, CA, Dec 2004.

Seong-Eun Park, Stoyan Jeliazkov, Joseph J. Kopanski, John Suehle, and Eric Vogel, Albert Davydov, and Hyun-Keel Shin, "Electrical Characterization of MOS structures and Wide Bandgap Semiconductors by Scanning Kelvin Probe Microscopy", 2005 MRS Spring Meeting, San Francisco, CA .